What is claimed is:

1. In a semiconductor integrated circuit having means to lower an external supply voltage within a chip and to feed the lowered voltage to at least a part of internal circuitry;

a semiconductor integrated circuit characterized in that the feed means comprises means to produce an output voltage whose change versus the external supply voltage is not constant when said external supply voltage is changed from a lower limit value thereof in an ordinary operation range of the chip to a value thereof at an aging operation point of said chip.

2. A semiconductor integrated circuit according to Claim 1, wherein the change of the output voltage of said feed means is very small when said external supply voltage changes within the ordinary operation range.

3. A semiconductor integrated circuit according to Claim 1, wherein the change of the output voltage of said feed means follows up the change of said external supply voltage when said external supply voltage changes within the ordinary operation range.

4. A semiconductor integrated circuit according to any of Claims 1, 2 and 3, wherein said feed means changes its output voltage so as to reach unequal aging voltages in succession in accordance with the change of

said external supply voltage.

5. A semiconductor integrated circuit according to any of Claims 1, 2, 3 and 4, wherein said feed means comprises means to prevent its output voltage from exceeding a breakdown voltage of the internal circuit when said output voltage of said feed means has exceeded a predetermined aging voltage.

6. A semiconductor integrated circuit according to Claim 5, wherein said feed means comprises means to negatively change its output voltage in correspondence with raise of said external supply voltage when said output voltage of said feed means has exceeded the predetermined aging voltage.

Add D7